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filed application)

Application Number	10/017,201
Filing Date	December 14, 2001
First Named Inventor	Jeffrey D. Walker
Group Art Unit Number	3663
Examiner Name	Not yet known
Total Number of Pages in This Submission	7**
Attorney Docket Number	21153-05930

**ENCLOSURES (check all that apply)**

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- ☐ Power of Attorney
- ☐ Application Data Sheet
- ☒ Information Disclosure Statement & PTO-1449
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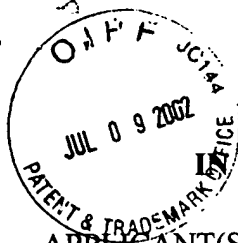
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GROUP 3600**REMARKS:** \*\* IDS references are not included in the total pages submitted.**SIGNATURE OF ATTORNEY OR AGENT**

Signature:		
Attorney/Reg. No.:	Michael Weber, Registration No. 50,951	Dated: June 28, 2002

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PATENT

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THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Jeffrey D. Walker et al.

APPLICATION NO.: 10/017,201

FILING DATE: December 14, 2001

TITLE: Optical Receiver Including Linear Semiconductor Optical Amplifier

CONFIRMATION NO: 6333

EXAMINER: Not yet known

GROUP ART UNIT: 3662

ATTY. DKT. NO.: 21153-05930

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Dated: June 28, 2002

By:

Michael Weber

Michael Weber, Registration No. 50,951

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INFORMATION DISCLOSURE STATEMENT

Under 37 CFR §§ 1.56 and 1.97-98

SIR:

Pursuant to the provisions of 37 CFR §§ 1.56 and 1.97-98, enclosed herewith is modified form PTO-1449 listing references for consideration by the Examiner.

The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

This Information Disclosure Statement is being filed:

- ☒ within three months of the filing date of the application, or date of entry into the national stage of an international application, or before the mailing date of a first office action on the merits, whichever event last occurred;
- ☐ before the mailing of a first official action after the filing of a request for continued examination (RCE) under 37 CFR § 1.114;
- ☐ after three months of the filing date of this national application or the date of entry of the national stage in an international application, or after the mailing date of the first official action on the merits, whichever event last occurred, but before the mailing date of the first to occur of either: (1) a final action under 37 CFR § 1.113; or (2) an action that otherwise closes prosecution in the application, and:
  - ☐ attached hereto is the fee set forth under 37 CFR § 1.17(p) for submission of this Information Disclosure Statement under 37 CFR § 1.97(c); OR
  - ☐ Applicant certifies pursuant to 37 CFR § 1.97(e) that:
    - ☐ each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; OR
    - ☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 CFR § 1.56(c) more than three months prior to the filing of this Statement;
- ☐ before the payment of the issue fee but after the mailing date of the first to occur of either: (1) a final action under 37 CFR § 1.113; or (2) an action that otherwise closes prosecution in the application, and:
  - ☐ Applicant certifies pursuant to 37 CFR § 1.97(e) that:
    - ☐ each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not

more than three months prior to the filing of this Statement;  
or

☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 CFR § 1.56(c) more than three months prior to the filing of this Statement; AND

☐ attached hereto is the fee set forth under 37 CFR §1.17(p) for submission of this Information Disclosure Statement under 37 CFR. § 1.97(c); OR

☐ after the payment of the issue fee. Applicant request that the information contained in this Information Disclosure Statement be placed in the file according to 37 CFR § 1.97(i), although the information may not be considered by the USPTO.

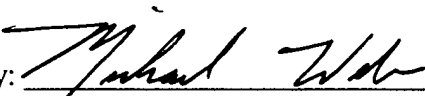
☒ This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application No. 10/014,679, filed on December 11, 2001, and the references cited therein are hereby referenced, but are not required to be provided in this application under 37 CFR § 1.98(d).

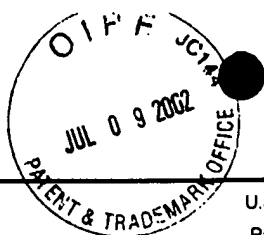
☒ Applicant submits that no fee is required for the consideration of this Information Disclosure Statement.

Consideration of the listed references and favorable action are solicited.

Respectfully submitted,  
JEFFREY D. WALKER et al.

Dated: June 28, 2002

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Patent and Trademark OfficeAttorney's Docket No.  
21153-05930Serial No.  
10/017,201**INFORMATION DISCLOSURE CITATION**

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Applicant  
Jeffrey D. Walker et al.Filing Date  
December 14, 2001Group Art Unit  
3663**U.S. PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	3,467,906	09/16/69	Cornely et al.	330	4.3	
	3,828,231	08/06/74	Yamamoto	357	30	
	4,794,346	12/27/88	Miller	330	4.3	
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	5,960,024	09/28/1999	Li et al.	372	96	
	6,044,100	03/28/2000	Hobson et al.	372	46	
	6,115,517	09-05-00	Shiragaki et al.	385	24	

**FOREIGN PATENT DOCUMENTS**

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	JP 01129483	11/14/87	Japan	H01S	3/18	No	
	JP 10190147	07/21/98	Japan	H01S	3/18	No	
	JP 56006492	01/23/81	Japan	H01S	3/18	No	

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

A	Alcatel, "Alcatel Optronics introduces a Gain-Clamped Semiconductor Optical Amplifier," <i>Press Release for Immediate Publication</i> , OFC '98, San Jose (Feb. 1998), 1 unnumbered page.
B	Bauer, B. et al., "Gain Stabilization of a Semiconductor Optical Amplifier by Distributed Feedback," <i>IEEE Photonics Technology Letters</i> , Vol. 6, No. 2 (Feb. 1994), pages 182-185.
C	Dorgeuille, F., et al., "1.28 Tbit/s Throughput 8x8 Optical Switch Based on Arrays of Gain-Clamped Semiconductor Optical Amplifier Gates," <i>Optical Fiber Communication Conference</i> , Vol. 4, Pages 221-223, March 2000.
D	Dorgeuille, F., et al., H., "Fast Optical Amplifier Gate Array for WDM Routing and Switching Applications," <i>OFC '98 Technical Digest</i> , Pages 42-44, 1998.
E	Doussiere, P. et al., "Clamped Gain Travelling Wave Semiconductor Optical Amplifier for Wavelength Division Multiplexing Applications," Maui, Hawaii, Sept. 19-23, 1994, New York, IEEE, US, Vol. Conf. 14 (9/14/94), pages 185-186.
F	Evankow, Jr., J.D., et al., "Photonic Switching Modules Designed with Laser Diode Amplifiers," <i>IEEE, Journal on Selected Areas in Communications</i> , Vol. 6, No. 7, Pages 1087-1095, August 1988.

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DATE CONSIDERED

EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered.

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Attorney's Docket No.  
21153-05930

Serial No.  
10/017,201

Applicant  
Jeffrey D. Walker et al.

Filing Date  
December 14, 2001

Group Art Unit  
3662

## U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

## FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation
					Yes No

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

G	Gee, S. et al., "High-Power Mode-Locked External Cavity Semiconductor Laser Using Inverse Bow-Tie Semiconductor Optical Amplifiers," <i>IEEE Journal of Selected Topics in Quantum Electronics</i> , Vol. 4, No. 2, March/April 1998, pages 209-215.
H	Jeong, G., et al., "Gain Optimization in Switches Based on Semiconductor Optical Amplifiers," <i>Journal of Lightwave Technology</i> , Vol. 13, No. 4, Pages 598-605, April 1995.
I	Joyner, C.H. et al., "Extremely Large Band Gap Shifts for MQW Structures by Selective Epitaxy on SiO <sub>2</sub> Masked Substrates," <i>IEEE Photonics Technology Letters</i> , Vol. 4, No. 9 (Sept. 1992), pp. 1006-1009.
J	Kitamura, S., et al., "Spot-Size Converter Integrated Semiconductor Optical Amplifiers for Optical Gate Applications," <i>IEEE Journal of Quantum Electronics</i> , Vol. 35, No. 7, Pages 1067-1074, July 1999.
K	Koyama, F., et al., "Multiple-Quantum-Well GaInAs/GaInAsP Tapered Broad-Area Amplifiers with Monolithically Integrated Waveguide Lens for High-Power Applications," <i>IEEE Photonics Technology Letters</i> (August 1993), Vol. 5, No. 8, pages 916-919.
L	Leuthold, J., et al., "All-Optical Space Switches with Gain and Principally Ideal Extinction Ratios," <i>IEEE Journal of Quantum Electronics</i> , Vol. 34, No. 4, Pages 622-633, April 1998.
M	McAdams, L.R. et al., "Linearizing High Performance Semiconductor Optical Amplifiers: Techniques and Performance," <i>LEOS Presentation</i> (1996), pages 363-364.
N	Mutalik, V.G. et al., "Analog performance of 1310-nm gain-clamped semiconductor optical amplifiers," <i>OFC '97 Technical Digest</i> , Thursday Morning, 11:15 AM, pages 266-267.
O	Simon, J.C. et al., "Travelling wave semiconductor optical amplifier with reduced nonlinear distortions," <i>Electronics Letters</i> , Vol. 30, No. 1 (Jan 6, 1994), pages 49-50.
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R	Tiemeijer, L.F. et al., "1310-nm DBR-Type MQW Gain-Clamped Semiconductor Optical Amplifiers with AM-CATV-Grade Linearity," <i>IEEE Photonics Technology Letters</i> , Vol. 8, No. 11 (Nov. 1996), pages 1453-1455.

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3662**U.S. PATENT DOCUMENTS**

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	Document Number	Date	Country	Class	Subclass	Translation	
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**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

S	Tiemeijer, L.F. et al., "High-Gain 1310 nm Semiconductor Optical Amplifier Modules with a Built-in Amplified Signal Monitor for Optical Gain Control," <i>IEEE Photonics Technology Letters</i> , Vol. 9, No. 3 (March 1997), pages 309-311.
T	Tiemeijer, L.F. et al., "Reduced Intermodulation Distortion in 1300 nm Gain-Clamped MQW Laser Amplifiers," <i>IEEE Photonics Technology Letters</i> , Vol. 7, No. 3 (March 1995), pages 284-286.
U	Toptchiyski, G., et al., "Time-Domain Modeling of Semiconductor Optical Amplifiers for OTDM Applications," <i>IEEE Journal of Lightwave Technology</i> , Vol. 17, No. 12, Pages 2577-2583, December 1999.
V	van Roijen, R., et al., "Over 15 dB Gain from a Monolithically Integrated Optical Switch with an Amplifier," <i>IEEE Photonics Technology Letters</i> , Vol. 5, No. 5, Pages 529-531, May 1993.
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